Amendments to the Claims:

A clean version of the entire set of pending claims, including amendments to the claims, is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Previously Presented) A method of operating a data-processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations, the method comprising: in performing cryptographic operations in the integrated circuit, at least two processors, CPU and co-processors, perform cryptographic operations simultaneously and in parallel, wherein the cryptographic operations of at least one processor, CPU or co-processor, are useful operations and the cryptographic operations performed by at least one other processor, CPU or co-processor, are dummy operations whose results are rejected, and consumption characteristics of the data-processing device being a superimposition of consumption characteristics associated with performing both useful and rejected cryptographic operations, whereby reconstruction of the consumption characteristics associated with performing any of the useful cryptographic operations is impeded.

3. (Previously Presented) A method as claimed in claim 2, wherein the selection as to which processor, CPU or co-processor, performs a useful operation is random-controlled.

4. (Previously Presented) A method as claimed in claim 2, wherein a cryptographic operation is split up into at least two sub-operations and at least two

processors perform at least one sub-operation in parallel and simultaneously with at least one dummy operation.

5. (Canceled)

6. (Previously Presented) A method as claimed in claim 4, characterized in that the selection as to which processor performs the at least one sub-operation in parallel and simultaneously with at least one dummy operation is random-controlled.

7. (Previously Presented) A method as claimed in claim 4, wherein subsequently corresponding sub-results from the respective sub-operations are combined to an overall result of the overall cryptographic operation.

8. (Original) A method as claimed in claim 7, characterized in that the split-up of the cryptographic operation into sub-operations is random-controlled.

9. (Previously Presented) A method as claimed in claim 7, characterized in that the sub-operations are parts of an encryption in accordance with Data Encryption Standard (DES).

10. (Previously Presented) A data-processing device with an integrated circuit, comprising: a central processing unit (CPU) and one or more co-processors, a control unit which controls the CPU and co-processors so that, in the case of a cryptographic operation, at least two of the CPU and co-processors perform a cryptographic operation simultaneously and in parallel with at least one dummy operation, whereby consumption characteristics associated with performing the respective cryptographic and dummy operations are superimposed so that reconstruction of the consumption characteristics associated with performing the cryptographic operation is impeded.

11. (Previously Presented) A data-processing device as claimed in claim 10, wherein the control unit comprises a splitter which splits a cryptographic operation into at least two sub-operations, and at least one of the sub-operations and at least one dummy operation is supplied for simultaneous processing to two separate of the CPU and co-processors.

12. (Previously Presented) A data-processing device as claimed in claim 11, wherein the control unit further comprises a recombiner which recombines each sub-result of the sub-operations simultaneously performed by the CPU and co-processors and the at least one dummy operation results are rejected to an overall result of the overall cryptographic operation.

13. (Previously Presented) A data-processing device as claimed in claim 12, wherein the splitter splits a cryptographic operation so that at least one sub-operation is a dummy operation, and wherein the recombiner rejects the relevant result of a processor that has performed such dummy operation.

14. (Previously Presented) A data-processing device as claimed in claim 13, further comprising a random generator which is connected to the splitter so that the splitter operates in a random-controlled manner.

15-28. (Canceled)